CLAIMS

1. A level shifter device having a single-ended input comprising:

a first transistor device coupled to at least the input and adapted to have a threshold voltage less than 0V;

a second transistor device coupled to at least said first transistor device; and

a level shifter transistor device coupled to at least said first and second transistor devices.

2. The circuit of Claim 1, wherein said first transistor device comprises a native NMOS transistor device adapted to have a threshold voltage less than 0V over all operating conditions of the level shifter circuit.

3. The circuit of Claim 1, wherein said second transistor device comprises a PMOS transistor device.

4. The circuit of Claim 3, wherein said PMOS transistor device has a gate coupled to an output.

5. The circuit of Claim 1, wherein said level shifter transistor device comprises at least a PMOS transistor device.

6. The circuit of Claim 1, wherein said level shifter transistor device comprises at least one NMOS transistor device.

7. The circuit of Claim 1, wherein said level shifter transistor device comprises PMOS and NMOS transistor devices coupled to at least an output.

8. A multi-level level shifter circuit device having a single-ended input comprising:

a first NMOS transistor device coupled to at least the input and adapted to have a threshold voltage less than 0V;

a first PMOS transistor device coupled to at least said first NMOS device and an output;

a second PMOS transistor device coupled to at least said output and said first NMOS and first PMOS transistor devices; and

a second NMOS transistor device coupled to at least said output and said first NMOS and second PMOS transistor devices.

9. A method of translating a voltage level a single-ended input signal comprising:

outputting a first voltage level if the single ended input signal is in a first state; and

outputting a second voltage level if the single ended input is in a second state.

10. The method of Claim 9, wherein said first state comprises a high state.

11. The method of Claim 9, wherein said second state comprises a low state.

12. The method of Claim 9, wherein said first voltage level comprises a high signal.

13. The method of Claim 9, wherein said second voltage level comprises a low signal.

14. The method of Claim 9, wherein said first voltage level comprises a low signal.

15. The method of Claim 9, wherein said second voltage level comprises a high signal.

16. A method of translating a voltage level of a single-ended input signal comprising:

determining if the input signal is high;

outputting a low signal if the input signal is high; and

outputting a high signal if the input signal is not high.

17. The method of Claim 16, wherein determining if the input signal is high comprises determining if the input signal is greater than a first voltage.

18. The method of Claim 16, wherein determining if the input signal is not high comprises determining if the input signal is less than a second voltage.

19. The method of Claim 16, further comprising eliminating static current drain.

20. A method of translating a voltage of an input signal from one level to another using a single-ended input comprising:

determining if the input signal is greater than a threshold value of a transistor device;

outputting a low signal if the input signal is greater than said threshold value;

outputting a high signal if the input signal is not greater than said threshold value; and eliminating static current drain.